Digital and Analog ASICs

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Market Trends and Strategy in ASIC

- Cloud computing will fuel the next wave, generating increasing demand for (green) infrastructure and transforming all applications in cloud conscious clients.
- ASIC continues to be an effective win-win model for CCI customers and ST continuses to be committed to it.
- The strategy: expanded product offering and flexible business model.

CCI Performance Through the Crisis

- Back to Growth
- Accelerating Margins
- Reducing Dependency
- Expanding New Business
Leading by Technology Acceleration

System-On-Chip

Motor Controllers, Head Drivers

CCI Growth Drivers

- BiCMOS ASIC for AOC and RF
- Digital ASIC for Networking
- PrintHeads for InkJet Printers
- Printer SOC and SPEAr eMPU
BiCmos ASICs for Networking

- Leveraging best-in-class BiCmos technologies from ST technology portfolio
  - BiCmos7RF: State-of-the-art performances for both noise and linearity
  - BiCmos9MW: 100G Ethernet Optical Link successfully demonstrated
- Consolidating ST presence in RF COTs for application in wireless base-stations
- Growing in the area of active cables

PrintHeads for InkJet Printers

- Expanding ST leadership in thermal printheads
- Best-in-class microfluidic technology
- Strategic partnerships with multiple customers
- Revenue growth very material in 2009
- Investing in Piezo technology to address new markets
STMicroelectronics Announces 32nm Design Platform for Next-Generation System-on-Chip ICs for Networking Applications

Geneva, May 25, 2010 - STMicroelectronics (NYSE: STM), a world leader in high-performance System-on-Chip (SoC) ICs, today announced full availability of a 32-nanometer (nm) technology platform for the design and development of leading-edge application-specific integrated circuits (ASICs) for networking applications. Central to the new 32nm SoC design platform, which implements ST’s 32LPH (Low-Power High-performance) process technology, is the industry’s first Serializer-Deserializer (SerDes) IP available in 32nm ‘bulk’ silicon.

Enabling very large ASIC designs, greater than 200mm², ST’s new 32nm 32LPH ASIC design platform enables an unprecedented mix of high performance, high complexity, low power consumption and reduced silicon real estate per functional block. The platform is designed to accelerate the development of next-generation networking ASICs used in high-performance applications such as enterprise switches, routers and servers as well as optical cross-connect and wireless infrastructure applications.

“With the introduction of the 32LPH platform, ST is enabling the next generation of equipment for communication infrastructure applications, which requires highly integrated ASICs that can satisfy the increasing demand in performance, while also meeting extremely challenging power consumption and silicon integration goals,” said Riccardo Ferrari, Group Vice President and General Manager of ST’s Networking and Storage Division. “We are extremely encouraged by the strong interest that customers are demonstrating for this platform, which has already gained key design wins.”

ST’s SerDes IP, called S12, is a key piece of intellectual property that has already been successfully demonstrated in labs at selected key customers. The S12 IP is vital for the development of ASICs for networking applications and enables chip-to-chip, chip-to-module and backplane communications in networking equipment designs.

“ST is the first silicon supplier to bring a full design platform in a 32nm bulk-silicon process technology to the communication infrastructure market, including a next-generation predictive ASIC top-down design methodology, together with a full set of proven IP, such as a SerDes and embedded DRAM, successfully developed over many years by ST in previous technology nodes,” said Philipp Maganishvili, Technology R&D Group Vice-President, Central CAD & Design Solutions GM, STMicroelectronics. “ST’s Technology R&D center in Crolles, France, has been instrumental in accelerating the completion of the 32LPH platform where low-power technology meets the high-performance requirements of networking applications, while still enjoying all the cost benefits of high-volume manufacturing. In addition, we have partnered with selected EDA vendors to offer networking customers the benefits of a predictable ASIC turnaround time, including fast virtual physical prototyping, and 32nm-class timing, signal and power integrity sign-off.”

The first ASIC prototypes implemented in ST’s 32LPH process technology are expected early in 2011 with production ramp-up in the second half of 2011.

Further Technical Information

ST’s 32LPH (Low-Power High-performance) design platform for networking applications supports up to 10 metallization layers to increase routing efficiency. The platform is based on the 32nm High-K Metal Gate process developed within the framework of the ISDA alliance, but also incorporates specific IP and devices from ST, such as embedded DRAM with 10-Mbit per square millimeter density and Ternary Content Address Memory (TCAM).
Printer SOC and SPEAr

- SPEAr family now expanding with the launch of the 1300 series
- Enabling flexible ASIC models into multiple applications
- Decreasing cost of ownership to customers
- State-of-the-art SOC architecture
- Anticipating continuous growth moving forward fueled by recent wins in printer SOCs and increasing revenues from the SPEAr family

SPEAr Enables Multiple Business Models

- Traditional ASIC
- Flexible ASIC
- Embedded Processing

Decreasing Cost of Ownership to Customers
STMicroelectronics Expands its SPEAr® Microprocessor Family for High-Performance Applications

Geneva, May 27, 2010 - STMicroelectronics (NYSE: STM), a world leader in system-on-chip technology, today revealed the new architecture that will be the backbone for the new members of its popular SPEAr® (Structured Processor Enhanced Architecture) family of embedded microprocessors, targeting high-performance connectivity and embedded applications.

Leveraging its experience of the production-proven SPEAr300 and SPEAr600 lines, the new SPEAr1300 product line couples powerful dual ARM Cortex-A9 processors with a DDR3 memory interface and is manufactured in ST’s low-power 55nm HCMOS (high-speed CMOS) process technology. The dual ARM Cortex-A9 processors support fully symmetrical operation, at speeds up to 600MHz/core for 3000 DMIPS equivalent.

The SPEAr1300 makes use of ST’s innovative Network-on-Chip technology for internal peripheral interconnect, assuring support for multiple different traffic profiles, while maximizing data throughput in the most cost-effective and power-efficient way. Initial sampling has already started to early adopters.

The new architecture offers industry-leading performance in terms of DMIPS/MHz and power consumption/DMIPS ratios, in addition to cost efficiency and customizability advantages. The availability of integrated DDR3 memory controller and a full set of connectivity peripherals like PCIe, SATA, USB and Ethernet, among other features, make the SPEAr1300 the ideal choice for high-performance applications including networking, thin client, videoconferencing, NAS (Network-Attached Storage), computer peripherals, and factory automation.

“This new architecture for the SPEAr family builds upon the unrivalled low power and multiprocessing capabilities of the ARM Cortex-A9 processor core” said Loris Valenti, General Manager of ST’s Computer Systems SoC Division. “Upcoming SPEAr embedded microprocessors will deliver an unprecedented combination of processing performance, memory throughput, flexibility and low power for next-generation connectivity appliances.”

Key features of the new SPEAr1300 architecture include:

- Dual ARM Cortex-A9 cores, running at 600MHz for 3000 DMIPS equivalent
- 64-bit AXI (AMBA3) bus Network-on-Chip technology
- DRAM and L2 cache with Error Correction Code (ECC)
- 533MHz 2-channel DDR3 memory controllers with ECC; 16-bit DDR2 also supported
- Accelerator coherence port
- Gigabit Ethernet
- PCIe 2.0 supporting 5 Gt/s (Gigatransfers/second)
- SATA II 3 Gbit/s
- USB 2.0
- 256-bit key hardware encryption/decryption
- 1.3 million gates of configurable logic

Embedded microprocessors from the new SPEAr1300 product line will be announced over the next few months, expanding ST’s SPEAr family and providing an extensive choice for leading customers.

Further information on ST’s SPEAr family of embedded microprocessor System-on-Chip ICs is available at www.st.com/spear

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**Expansion of SPEAr Family**

New advanced symmetrical multiprocessor architecture from ST delivers cost efficiency, computing power and customizability for multiple embedded applications.

**SPEAr Roadmap**

- **2A9-1300**
  - 1300k gates
  - Dual Cortex-A9
  - 600MHz
  - HD Display, 3x PCIe
  - 55nm HCMOS LP

- **SPEAr300**
  - General Purpose
  - External AMBA bus
  - Off the shelf eMPU

- **SPEAr310**
  - Communication

- **SPEAr320**
  - Automation

- **SPEAr320 VoIP Security**

- **SPEAr310 Communication**

- **SPEAr300**
  - VoIP Security

- **2A9-1300**
  - 1300k gates
  - Dual Cortex-A9
  - 600MHz
  - HD Display, 3x PCIe
  - 55nm HCMOS LP

- **SPEAr1300**
  - First eMPU with Dual Cortex A9 available in silicon
Addressing Multiple Applications

Key Takeaways

- CCI product group is delivering solid results
  - Revenues in excess of $1B
  - Operating margin in the low double-digit range

- CCI product strategy centered on traditional ASIC, flexible ASIC and eMPU

- Strategy to grow in Analog
  - Continue to be a market leader in motor controllers for HDD and printers, and in printheads for inkjet printers
  - Now accelerating BiCMOS ASICs for both active optical cables and RF interfaces

- Strategy to grow in Digital
  - Significant design wins in the areas of communication infrastructure and printers
  - Launch of the first 32nm bulk platform for networking applications
  - Expansion of the SPEAr family with the launch of the 1300 series
  - Tactical participation in HDD SOC